Amendments to the Specification

Page 1, before line 1 insert the following -- This application is a Divisional of U.S. Application No. 09/735,541, filed December 15, 2000 (now allowed), the teachings of which are incorporated herein by reference.

Page 2, second aragraph:

A ~~sauce~~ source electrode 108 and a drain electrode 109 are placed on the a-Si layer 106 and n^+ a-Si layer 107, and a source wire 110 is formed integrally with the source electrode 108 through the same process.

Page 2 third paragraph:

A TFT 111 is constituted by the gate electrode 102, a-Si layer 106, n^+ a-Si layer 107, ~~sauce~~ source electrode 108, and drain electrode 109, etc., arranged as described above.

Page 3, first paragraph:

Moreover, the connection electrode 115 is joined to the source signal input terminal 103 so that the ~~sauce~~ source wire 110 and the source signal input terminal 103 are connected to each other through the terminal contact hole 104. Moreover, the display electrode layer 116 and the drain electrode 109 are connected through the display contact hole 112.

Page 3, third paragraph:

(1) First, a metal thin film, composed of titanium (Ti), aluminum (Al), or chromium (Cr), etc., is formed on a washed glass substrate 101 by sputtering, etc. Then, a photolithographic technique, which carries out etching by using a mask that is formed by applying photoresist to the metal thin film and exposing and developing it, is used to simultaneously form the gate electrode 102, the gate wire connected to the gate electrode 102 and the ~~sauce~~ source signal input terminal 103.

Page 5, paragraph 3:

Then, on top of these layers, through a gate insulation film 207, are formed an a-Si layer 208a made of an amorphous silicon semiconductor layer, and an n^+a-Si layer 208b that is an amorphous silicon semiconductor layer to which impurities such as phosphor (P) are added so as to realize ohmic connections between the a-Si layer 208a and a ~~sauce~~ source electrode 209b as well as a drain electrode 210.

Page 5, paragraph 4:

Next, after a multi-layer structure film, such as an Al/Ti film, not shown, has been deposited on the a-Si layer 208a and n^+a-Si layer 208b that are the semiconductors, a source electrode 209b, a drain electrode 210 and a source wire 209 that serves as bus wiring for them are formed. Moreover, a TFT 211 is formed by the ~~sauce~~ source wire 209, a ~~sauce~~ source electrode 209b and a ~~sauce~~ source signal input terminal 209c that are integral with the ~~sauce~~ source wire 209 and a drain electrode 210.

Page 6, paragraph 1:

Next, an overcoat layer 212, made of an insulation film such as SiN, for protecting the ~~sauce~~ source wire 209 and TFT 211, and a resin insulation film 213 made of an insulation photosensitive acrylic resin, etc. are successively laminated so that an overcoat layer having a two-layer structure is formed.

Page 6, paragraph 2:

Next, the resin insulation film 213, made of a photosensitive acrylic resin, etc., is exposed in an exposing process by using a predetermined mask, and then subjected to a developing process so that a contact hole 215 is formed in the resin insulation film 213. Simultaneously with this process, the resin insulation film 213 over the ~~sauce~~ source signal input terminal 209c, the gate signal input terminal 202a and support capacitor signal input terminal 204a is removed therefrom.

Page 6, paragraph 3:

By using the resin insulation film 213 thus patterned as a mask for an etching

process, the overcoat layer 212 located at the bottom of the contact hole 215, and the overcoat layer 212 covering the ~~sauce~~ source signal input terminal 209c, the gate signal input terminal 202a and the supplementary capacitance signal input terminal 204a are simultaneously removed.

Page 26, paragraph 3:

As illustrated in Fig. 1(a) and Fig. 1(b), the above-mentioned liquid crystal display has a TFT array substrate that is constituted by: a gate wire 2 formed on an insulation substrate 1 made of glass, etc., a ~~sauce~~ source wire (wiring) 3 that is orthogonal to the gate wire 2, a gate signal input terminal 2a that is connected to the gate wire 2 so as to supply signals from outside to the gate wire 2, a ~~sauce~~ source signal input terminal section 5 for supplying signals from an external driving circuit to the source wire 3, a TFT 6 that is placed in each pixel as a switching element in a matrix format, and a pixel display electrode 7 (in the Figure, indicated by an alternate long and two short dashes line) that is connected to each TFT 6 and that is made of ITO (Indium Tin Oxide)}.

Page 27, paragraph 3:

An explanation will be given of a specific construction of the ~~sauce~~ source signal input terminal section 5. First, a ~~sauce~~ source signal input terminal (terminal section)10, made from the same material as that of the gate wire 2 and the gate electrode 2b, is placed on the insulation substrate 1. An island-shape semiconductor layer (film, semiconductor layer) 11 is placed between the source signal input terminal 10 and the source wire 3 at their mutually overlapped portion (connection portion) between the ~~sauce~~ source signal input terminal 10 and the ~~sauce~~ source wire 3. This island-shape semiconductor layer 11 is constituted by a lower layer 11a and an upper layer 11b. The lower layer 11a is made from the same material as an a-Si layer forming the TFT6, which will be described later, and the upper layer 11b is made from the same material as an n^+a-Si layer forming the TFT6, which will be described later. Moreover, the source signal input terminal section 5 is coated with a protective film which will be described later; and in this protective film is formed a terminal section contact hole (contact hole) 12 which is used for connecting the source wire 3 and the source signal input terminal 10 of the connection portion by a connection electrode (connecting conductive film) 13 (indicated by an alternate long and two short dotted line, in the Figure) made from the same material as that of the pixel display electrode 7.

Page 29, paragraph 5:

In the ~~sauce~~ source signal input terminal section 5, the gate insulation film 16 is formed on the connection end 10a of the source signal input terminal 10 placed on the insulation substrate 1, and on the gate insulation film 16 are further placed the lower layer 11a of the island-shape semiconductor layer 11 made from the same material as the a-Si layer 8 and the upper layer 11b of the island-shape semiconductor layer 11 made from the same material as an n^+a-Si layer 9. As described earlier, the island-shape semiconductor layer 11 is placed beneath the connection end of the source wire 3 that provides connections to the source signal input terminal 10.

Page 39, paragraph 2:

Moreover, preferably, the ~~sauce~~ source wire 3 is extended 0.5 to 10μm from the periphery of the terminal section contact hole 12 to the inside of the terminal section contact hole 12, and the island-shape semiconductor layer 11 is designed in a manner so as to further extend 0.5 to 10μm to the inside of the terminal section contact hole 12.

Page 31, paragraph 2:

(1) First, a metal thin film (a single layered film, or a multi-layered film), composed of a conductor material, such as titanium (Ti), aluminum (Al), or chromium (Cr), etc., is formed on a washed insulation substrate 1 by sputtering, etc. Then, a photolithographic technique, which carries out etching by using a mask that is formed by applying photoresist to the metal thin film and exposing and developing it, is used to simultaneously form a gate electrode 2b, a gate wire 2 connected to the gate electrode 2b, a gate signal input terminal 2a connected to the gate wire 2 and a ~~sauce~~ source signal input terminal 10 which is connected to a source wire 3 in a process later.

If the examiner would prefer, applicants will provide a substitute specification with the above amendments incorporated upon request.